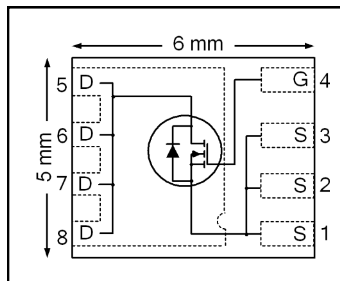
International
IOR Rectifier

# StrongIRFET™
# IRFH7084PbF

HEXFET® Power MOSFET

## Application
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC converters
- DC/AC Inverters




| | | |
|---|---|---|
| $V_{DSS}$ | | 40V |
| $R_{DS(on)}$ typ. | | 0.95mΩ |
| | max | 1.25mΩ |
| $I_D$ (Silicon Limited) | | 265A① |
| $I_D$ (Package Limited) | | 100A① |

## Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

PQFN 5X6 mm

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRFH7084PbF | PQFN 5mm x 6mm | Tape and Reel | 4000 | IRFH7084TRPbF |

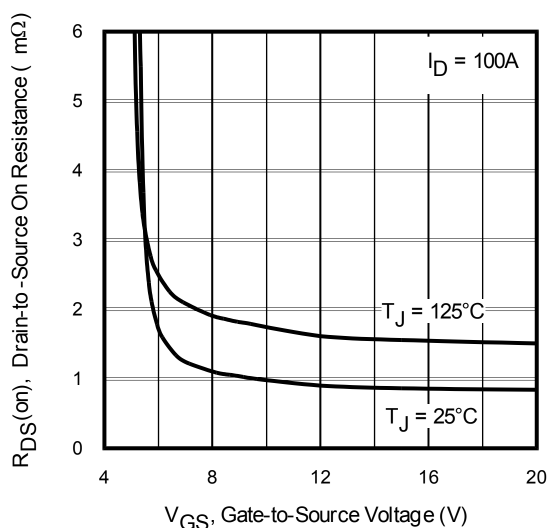



**Fig 1.** Typical On-Resistance vs. Gate Voltage

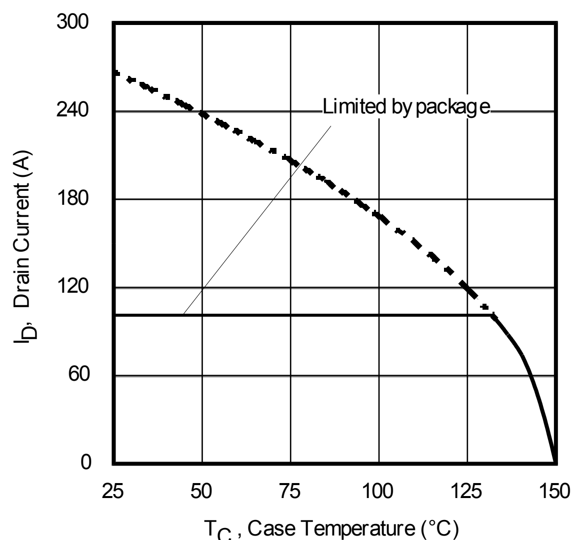



**Fig 2.** Maximum Drain Current vs. Case Temperature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### Absolute Maximum Rating

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_A$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 40 | A |
| $I_D$ @ $T_{C(Bottom)}$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 265① | |
| $I_D$ @ $T_{C(Bottom)}$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 170① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited) | 100① | |
| $I_{DM}$ | Pulsed Drain Current ① | 400 | A |
| | Linear Derating Factor | 1.25 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |

### Avalanche Characteristics

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ③ | 185 | mJ |
| $E_{AS\ (tested)}$ | Single Pulse Avalanche Energy Tested Value ⑨ | 370 | |
| $I_{AR}$ | Avalanche Current ② | See Fig 14, 15, 23a, | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |

### Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ (Bottom) | Junction-to-Case ⑧ | 0.5 | 0.8 | °C/W |
| $R_{\theta JC}$ (Top) | Junction-to-Case ⑧ | —— | 21 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑩ | —— | 35 | |
| $R_{\theta JA}$ (<10s) | Junction-to-Ambient ⑩ | —— | 20 | |

### Static @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.034 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 0.95 | 1.25 | mΩ | $V_{GS}$ = 10V, $I_D$ = 100A |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.2 | —— | 3.9 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 150μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 1.0 | μA | $V_{DS}$ =40 V, $V_{GS}$ = 0V |
| | | —— | —— | 150 | | $V_{DS}$ =40V, $V_{GS}$ = 0V, $T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Gate Resistance | —— | 1.4 | —— | Ω | |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability.
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.037mH, $R_G$ = 50Ω, $I_{AS}$ = 100A, $V_{GS}$ =10V.
④ $I_{SD} \leq$ 100A, di/dt $\leq$ 994A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.
⑤ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.
⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.
⑨ This value determined from sample failure population, starting $T_J$ =25°C, L=0.037mH, $R_G$ = 50Ω, $I_{AS}$ =100A, $V_{GS}$ =10V.
⑩ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf

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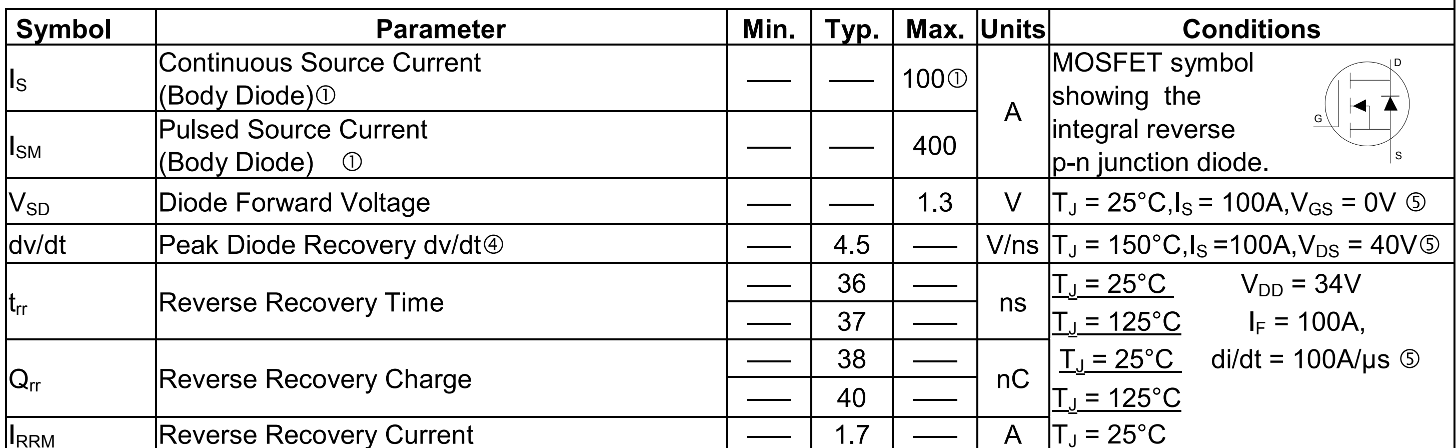
**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 120 | —— | —— | S | $V_{DS}$ = 10V, $I_D$ =100A |
| $Q_g$ | Total Gate Charge | —— | 127 | 190 | nC | $I_D$ = 100A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 35 | —— | | $V_{DS}$ = 20V |
| $Q_{gd}$ | Gate-to-Drain Charge | —— | 41 | —— | | $V_{GS}$ = 10V |
| $Q_{sync}$ | Total Gate Charge Sync. (Qg– Qgd) | —— | 195 | —— | | |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 16 | —— | ns | $V_{DD}$ = 20V |
| $t_r$ | Rise Time | —— | 31 | —— | | $I_D$ = 30A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 64 | —— | | $R_G$= 2.7Ω |
| $t_f$ | Fall Time | —— | 34 | —— | | $V_{GS}$ = 10V⑤ |
| $C_{iss}$ | Input Capacitance | —— | 6560 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 940 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 650 | —— | | ƒ = 1.0MHz, See Fig.5 |
| $C_{oss\ eff.(ER)}$ | Effective Output Capacitance (Energy Related) | —— | 1120 | —— | | $V_{GS}$ = 0V, VDS = 0V to 32V⑦ See Fig.11 |
| $C_{oss\ eff.(TR)}$ | Output Capacitance (Time Related) | —— | 1300 | —— | | $V_{GS}$ = 0V, VDS = 0V to 32V⑥ |

**Diode Characteristics**



| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode)① | —— | —— | 100① | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 400 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C,$I_S$ = 100A,$V_{GS}$ = 0V ⑤ |
| dv/dt | Peak Diode Recovery dv/dt④ | —— | 4.5 | —— | V/ns | $T_J$ = 150°C,$I_S$ =100A,$V_{DS}$ = 40V⑤ |
| $t_{rr}$ | Reverse Recovery Time | —— | 36 | —— | ns | $T_J$ = 25°C $V_{DD}$ = 34V |
| | | —— | 37 | —— | | $T_J$ = 125°C $I_F$ = 100A, |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 38 | —— | nC | $T_J$ = 25°C di/dt = 100A/μs ⑤ |
| | | —— | 40 | —— | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | —— | 1.7 | —— | A | $T_J$ = 25°C |



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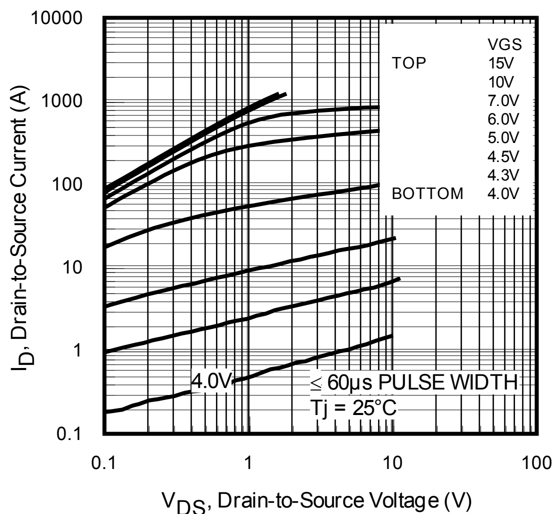


**Fig 3.** Typical Output Characteristics

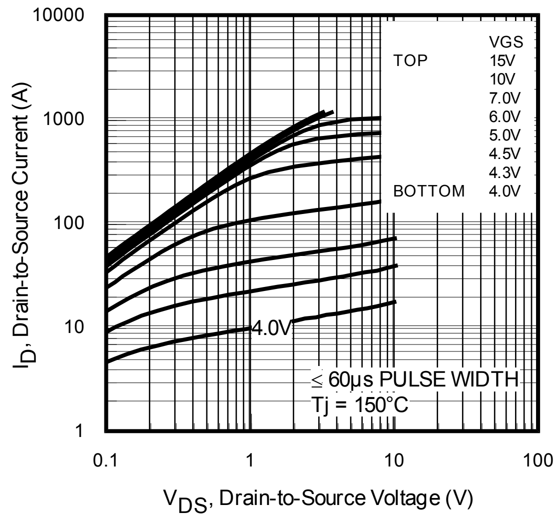


**Fig 4.** Typical Output Characteristics

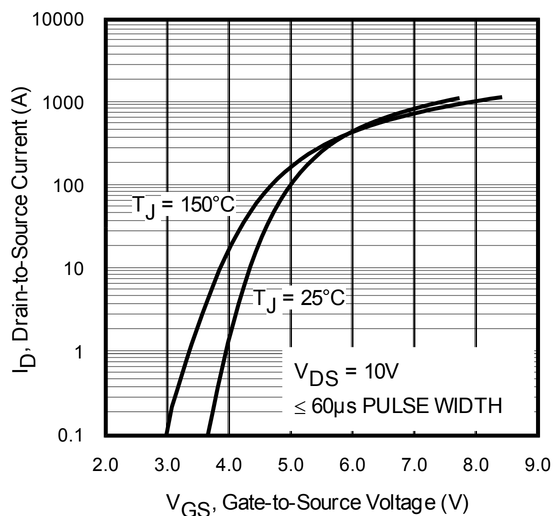


**Fig 5.** Typical Transfer Characteristics

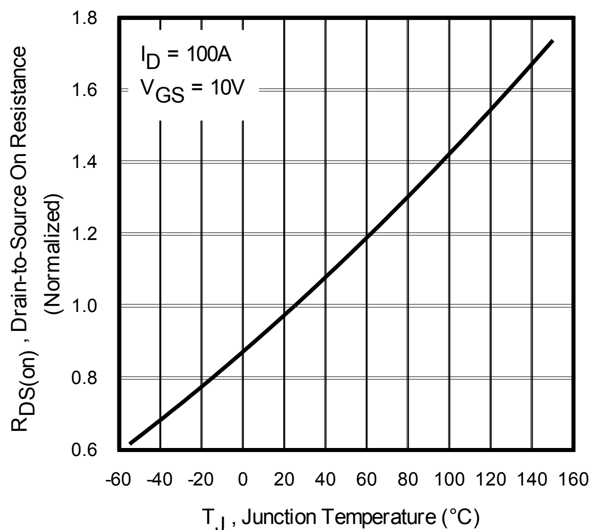


**Fig 6.** Normalized On-Resistance vs. Temperature

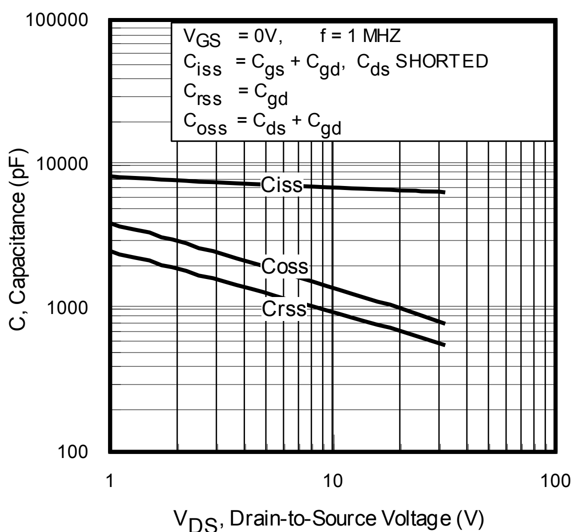


**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

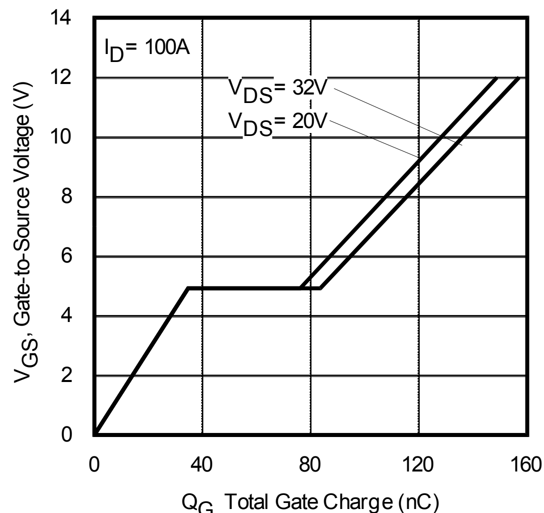


**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

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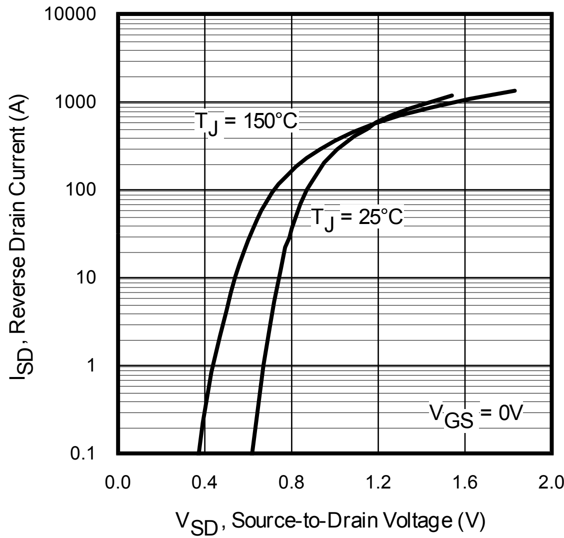


**Fig 9.** Typical Source-Drain Diode Forward Voltage

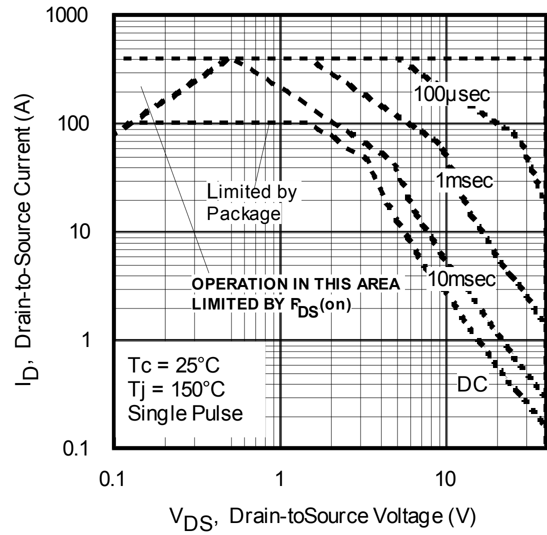


**Fig 10.** Maximum Safe Operating Area

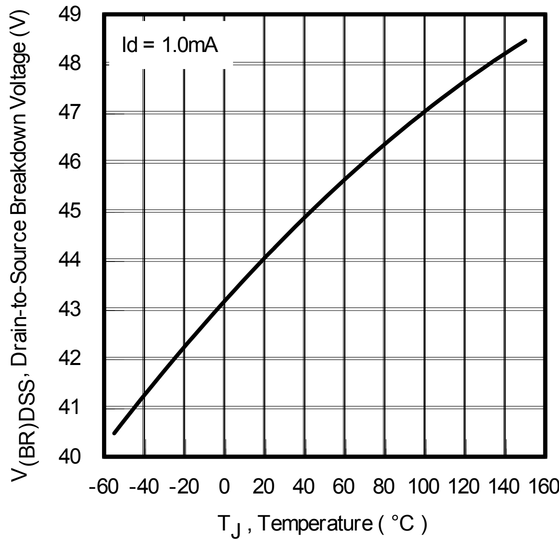


**Fig 11.** Drain-to–Source Breakdown Voltage

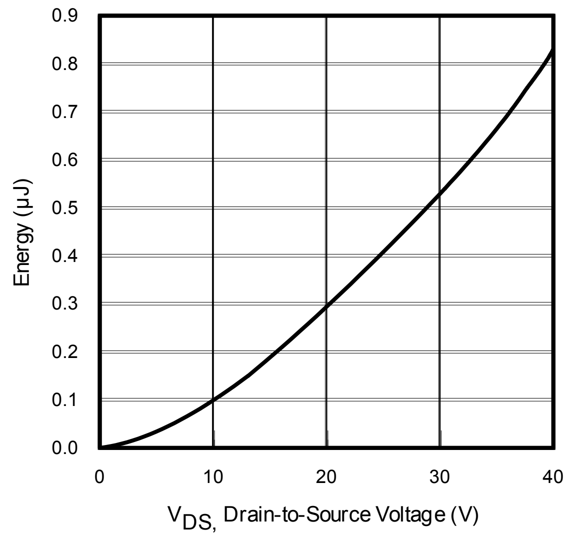


**Fig 12.** Typical $C_{oss}$ Stored Energy

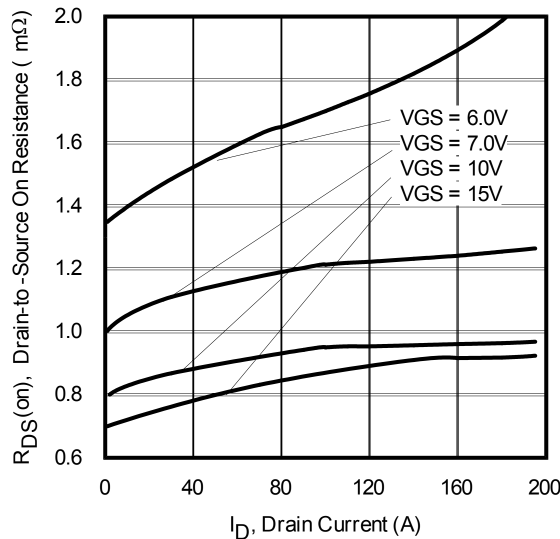


**Fig 13.** Typical On-Resistance vs. Drain Current

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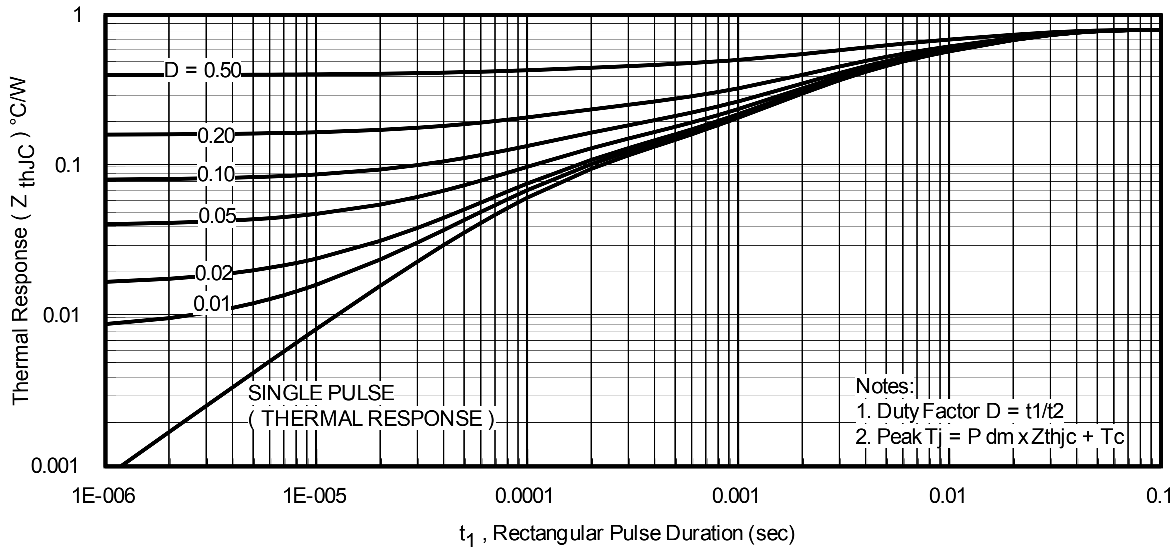


**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

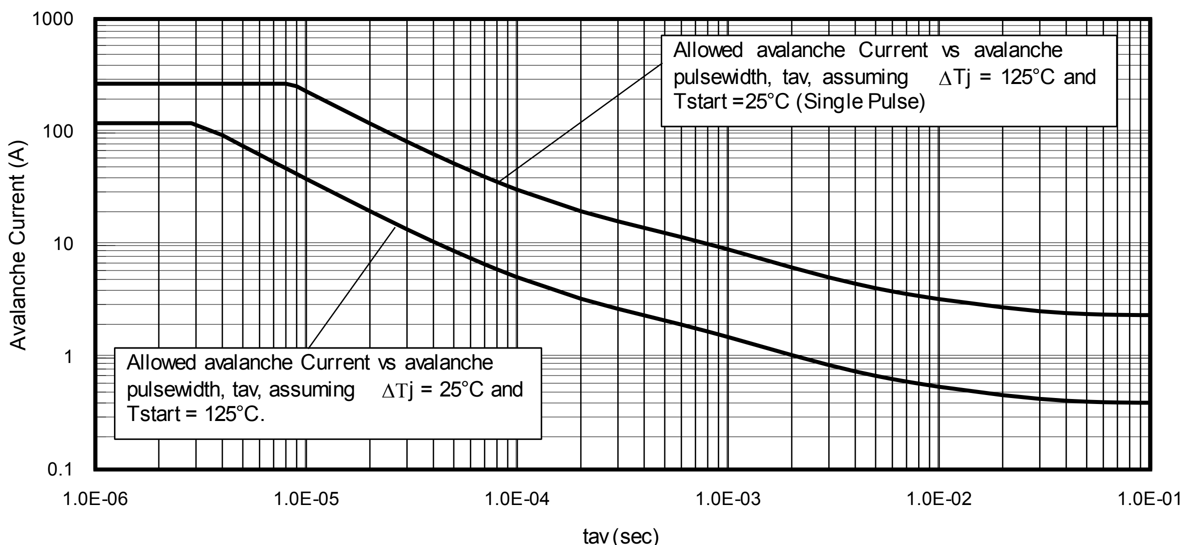


**Fig 15.** Typical Avalanche Current vs. Pulse width

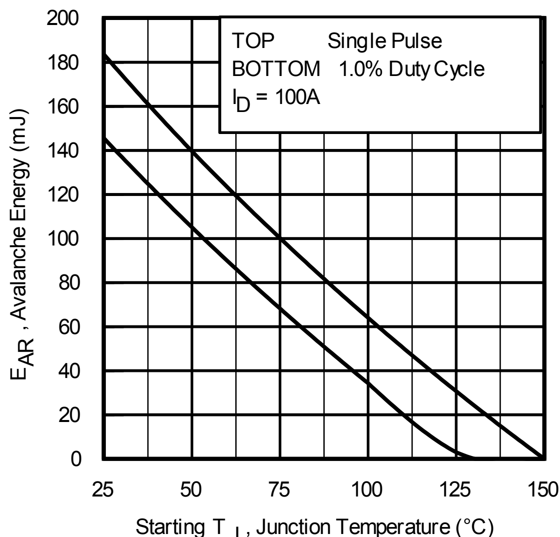


**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. $I_{av}$ = Allowable avalanche current.

7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 14, 15).

$t_{av}$ = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

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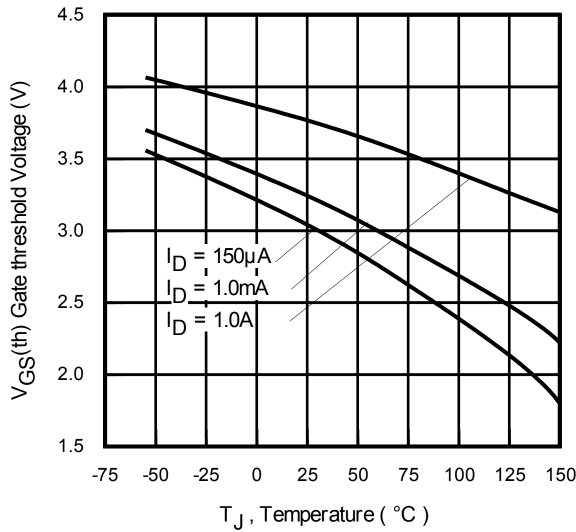


**Fig 17.** Threshold Voltage vs. Temperature

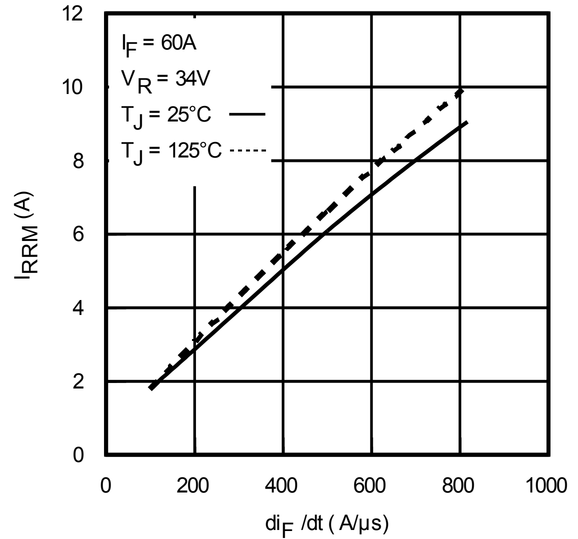


**Fig 18.** Typical Recovery Current vs. dif/dt

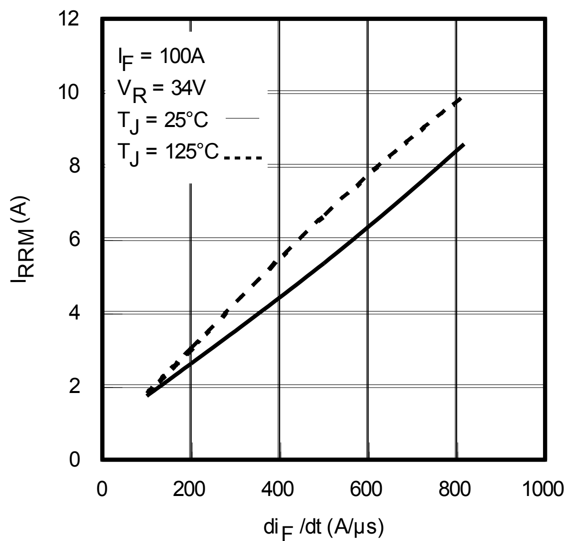


**Fig 19.** Typical Recovery Current vs. dif/dt

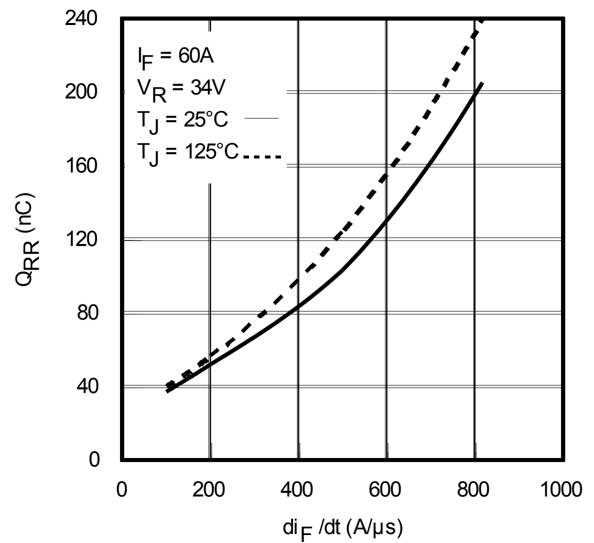


**Fig 20.** Typical Stored Charge vs. dif/dt

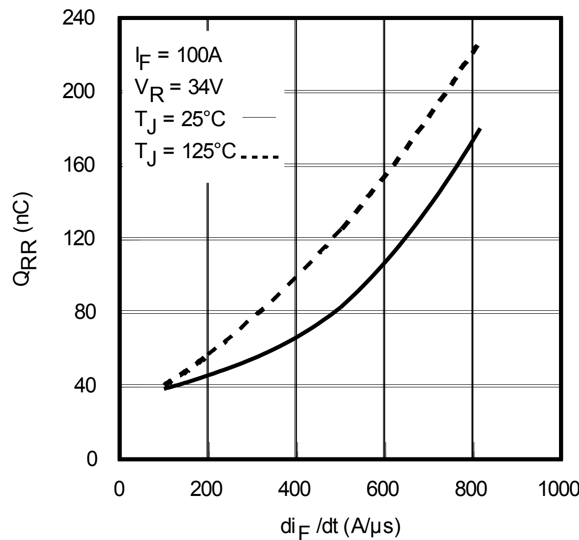


**Fig 21.** Typical Stored Charge vs. dif/dt

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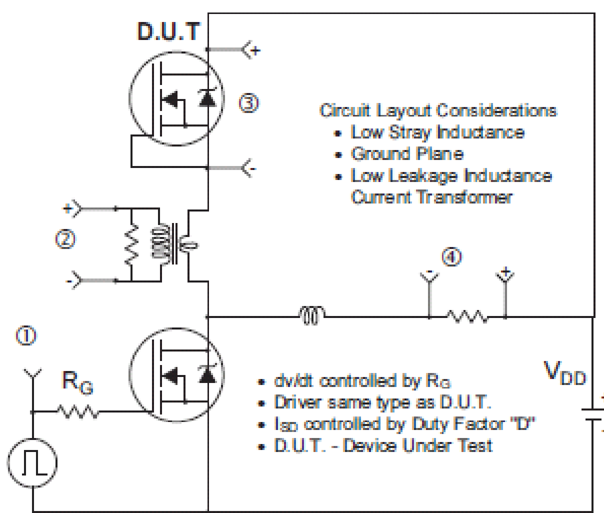


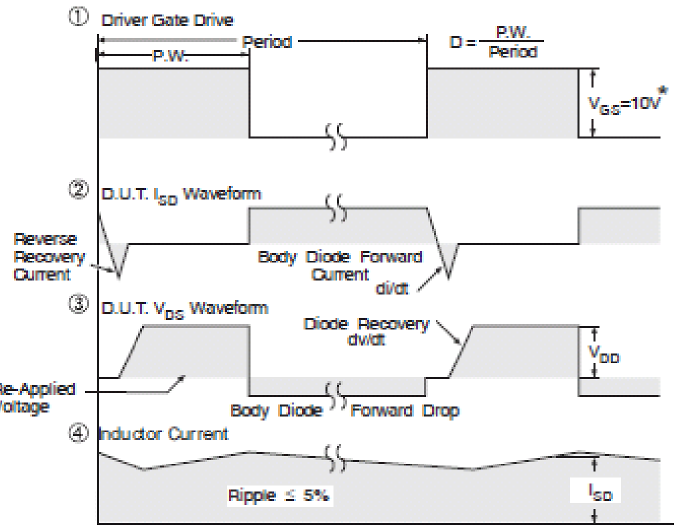


**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

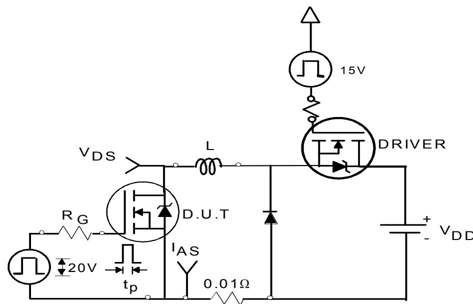


**Fig 23a.** Unclamped Inductive Test Circuit

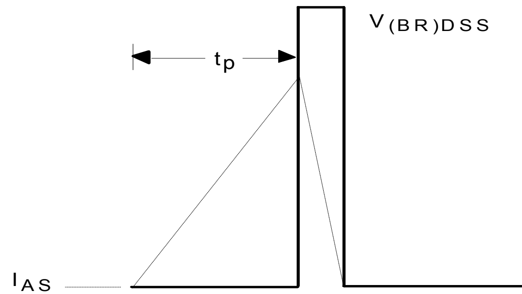


**Fig 23b.** Unclamped Inductive Waveforms

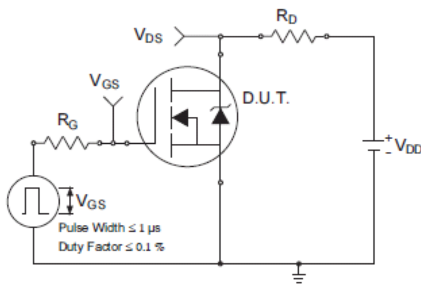


**Fig 24a.** Switching Time Test Circuit

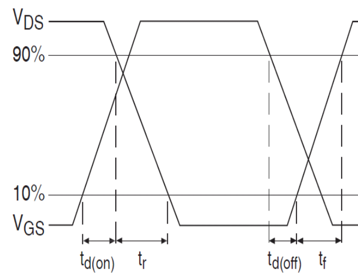


**Fig 24b.** Switching Time Waveforms

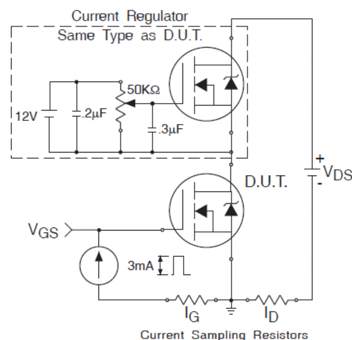


**Fig 25a.** Gate Charge Test Circuit

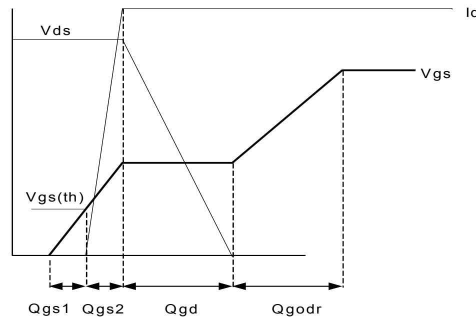


**Fig 25b.** Gate Charge Waveform

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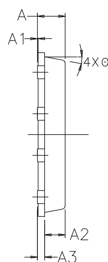
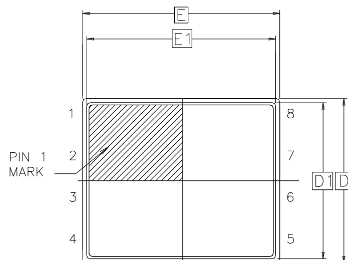
**PQFN 5x6 Outline "B" Package Details**

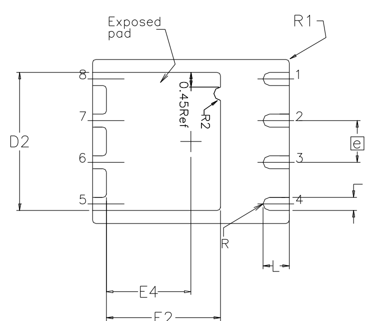



SIDE VIEW




TOP VIEW

| SYMBOL \ DIM | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.800 | 0.830 | 1.05 |
| A1 | 0.000 | 0.020 | 0.050 |
| A2 | 0.580 | 0.630 | 0.680 |
| A3 | | 0.254 REF | |
| θ | 0° | 10° | 12° |
| b | 0.350 | 0.400 | 0.470 |
| D | 4.850 | 5.000 | 5.150 |
| D1 | 4.675 | 4.750 | 5.000 |
| D2 | 3.700 | 4.210 | 4.300 |
| e | | 1.270 BSC | |
| E | 5.850 | 6.000 | 6.150 |
| E1 | 5.675 | 5.750 | 6.000 |
| E2 | 3.380 | 3.480 | 3.760 |
| E4 | 2.480 | 2.580 | 2.680 |
| L | 0.550 | 0.800 | 0.900 |
| R | | 0.200 REF | |
| R1 | | 0.100 REF | |
| R2 | 0.150 | 0.200 | 0.250 |

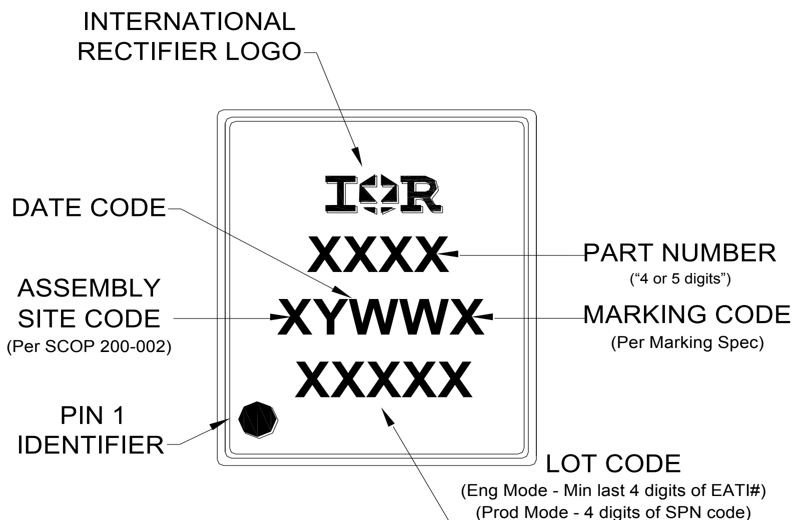



BOTTOM VIEW

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf

For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

**PQFN 5x6 Outline "B" Part Marking**




Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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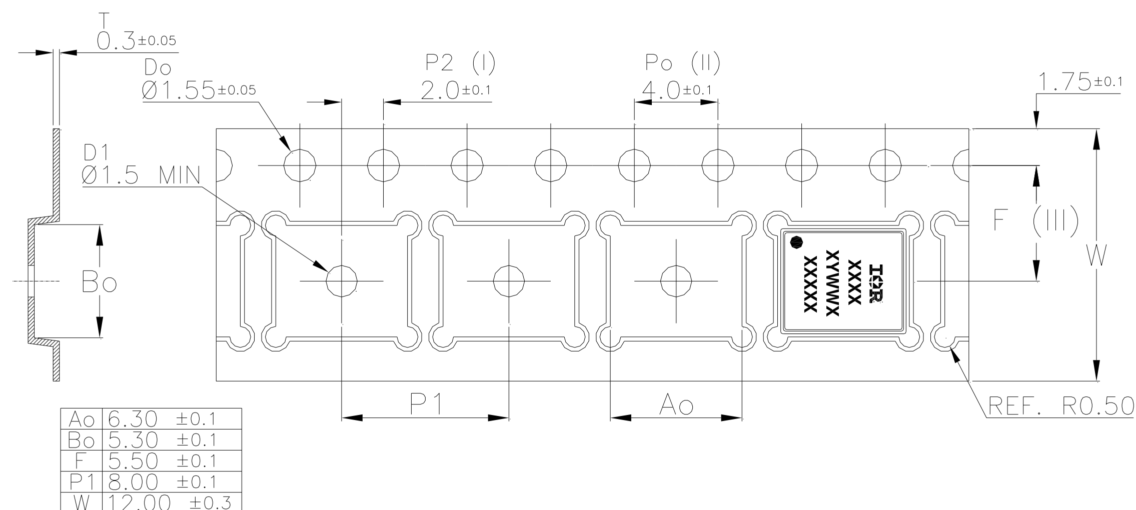
**PQFN 5x6 Outline "B" Tape and Reel**




Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

### Qualification information†

| | | |
|---|---|---|
| Qualification level | Industrial†† | |
| | (per JEDEC JESD47F ††† guidelines ) | |
| Moisture Sensitivity Level | PQFN 5mmx 6mm | MSL1 |
| | | (per JEDEC J-STD-020D††† ) |
| RoHS compliant | Yes | |

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

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